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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,841	10/01/2003	Jae-Yong Jeong	4591-348	9906

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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,841	JEONG ET AL.	
	Examiner	Art Unit	
	Pho M Luu	2824	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-16* is/are allowed.

6)☒ Claim(s) *1-3 and 7-10* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. Acknowledgment is made of applicant's Preliminary Amendment filed 17 November 2004. The changes and remarks disclosed therein were considered.

2. Claims 1-16 are pending in the application.

3. The corrected or substitute drawings were received on 17 November 2004 of Figure 6. This drawing is acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The

disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

6. The abstract of the disclosure is objected to because it uses the phrase **"Embodiments of the invention provide"** in line 6 and "**An embodiment's"** in line 8, which is implied. Correction is required. See MPEP § 608.01(b).

Claim Objections

7. Claim 2 is objected to because of the following informalities:

In claim 1, line 6: insert --a-- after "decoder units".

In claim 2, line 1: replace "claim 2" after memory device of with --claim 1--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3 and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwon. (US. 6,236,594).

Regarding claim 1, Kwon in Figures 1-2 disclosed a flash memory device (1, Figure 1) including a column pre-decode (Pre-decoder 12 including row and column, Figure 1) configured to control column selection transistor (selected transistors BT0-

BT17, Figure 2) that select a pre-determined bitline (BL0, BL1, Figure 2) from among a plurality of bitlines that are coupled to flash memory cells comprising:

a buffer unit (input/output Buffer 22 receive all input signal I/01-08, Figure 1) receives as input an all column selection signal;

decoder units (14, Figure 1-2) to decode an output of the buffer unit (14 select one of the memory blocks BLK0-BLKi in responsive to signal output from the Pre-decoder 12 and supply SSL, WLO-Wli, GSL) and a column address and

level shifters configured to generate column selection signal that are applied to gated (the gate of select transistor BTO-BT17 in Figure 2 are coupled to selected signal generator 15 to receive the block select signal BSELi, see column 2, lines 21-25) of the column selection transistor in response to an output of the decoder unit, wherein the level shifter are configured to apply a high voltage to all the column selection transistors during a stress test in response to the all column selection signal (see column 2, lines 8-39).

With respected to claim 2, Kwon in Figure 3 disclosed that the buffer unit comprises an inverter (106).

With respected to claim 3, Kwon in Figure 3 disclosed that each of the decoder units comprises an Nand gate (110) to receive as input the output of the buffer unit and the column address.

With respected to claim 7, Kwon in Figure 2 disclosed that the high voltage is provided directly from an external source (SSL, WL0-WL15, GSL of the selected memory block BT0-BT17 are driven with voltage VCC and VSS from drive circuit 16).

With respected to claim 8, Kwon in Figure 2 disclosed that the high voltage (program voltage Vpgm is 18V) has a voltage level higher than a power supply voltage (read voltage 4V, see column 5, lines 9-11).

With respected to claim 9-10, Kwon in Figure 3 disclosed that a constant voltage (program voltage is 18V and read voltage is 4V such as constant voltage apply during the operation) level is applied to the bitline during the strees test and a ground level voltage (VSS as ground level voltage).

Allowable Subject Matter

10. Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, the prior art of record do not disclose or suggest a second MOS transistor coupled between the drain of the second PMOS transistor and the ground voltage, with a gate coupled to the output of the decoder unit, and with a drain coupled to the drain of the second PMOS transistor to generate the column selection signal.

Regarding claim 5, the prior art of record do not disclose or suggest a second stage column selection transistor configured to select a pre-determined one of the at

least two bitlines in response to another group of the column selection signal and connect the predetermined one of the at least two bitlines with a data line.

Allowable Subject Matter

12. Claims 11-16 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "deactivating all the column selection signal and turning on selected ones of the column selection transistors in response to deactivating all the column selection signals by decoding a column address" as claimed in the independent claim 11.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Koh et al. (US. 5,654,925) disclosed a circuit applying a stress voltage for use in a semiconductor.

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
19 January 2005

VAN THU NGUYEN
PRIMARY EXAMINER